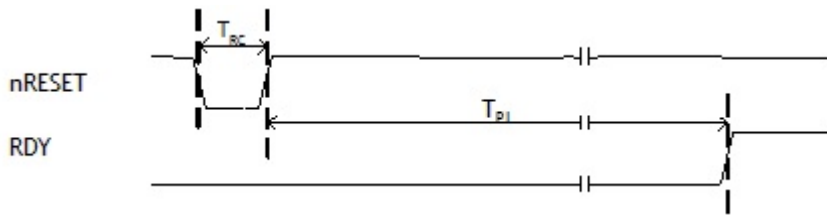


Table of Contents

Timing Diagram	1
Reset Timing	1
SPI Timing	1

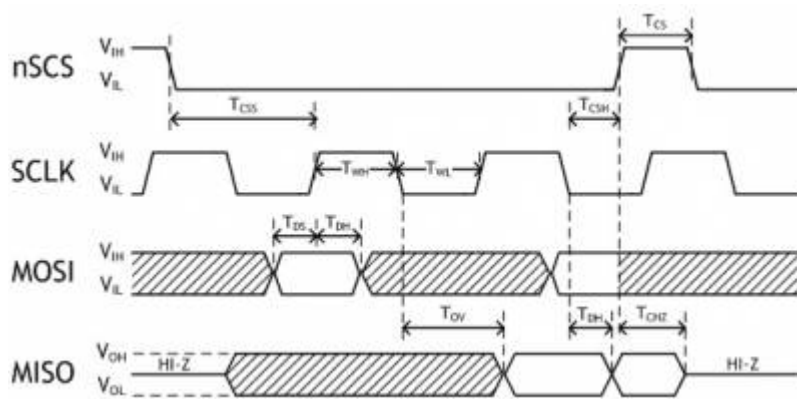
Timing Diagram

Reset Timing



Symbol	Description	Min	Max
TRC	Reset Cycle Time	500us	-
TPL	Internal Auto Configuration Time	-	50ms

SPI Timing



Symbol	Description	Min	Max	Units
Fsck	SCLK Clock Frequency	-	80	MHz
TWH	SCLK High duration	6	-	ns
TWL	SCLK Low duration	6	-	ns
TCS	nSCS High duration	5	-	ns

From:
<http://wizwiki.net/wiki/> -

Document Wiki

Permanent link:
<http://wizwiki.net/wiki/doku.php/products:wiz550io:timingdiagram>

Last update: 2015/03/16 10:33

