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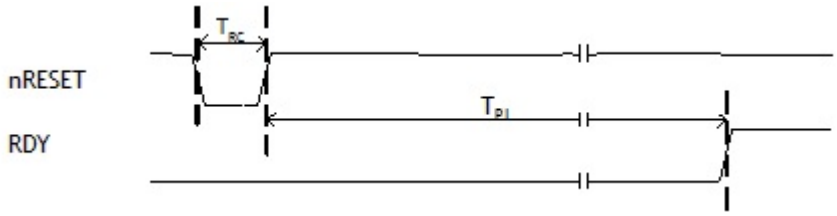
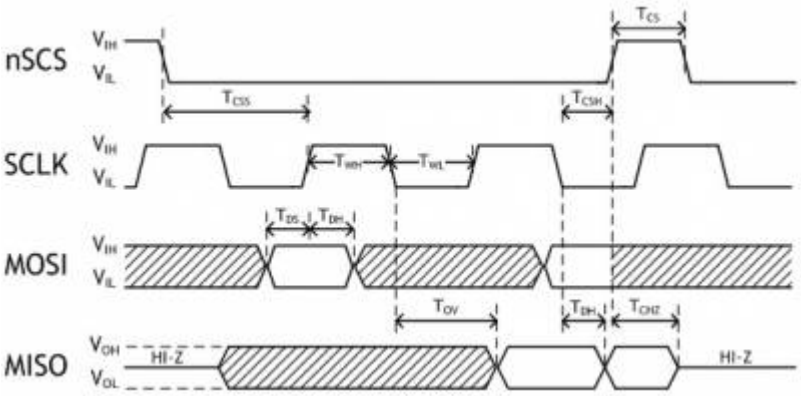
Timing Diagram

Reset Timing



Symbol	Description	Min	Max
TRC	Reset Cycle Time	500us	-
TPL	Internal Auto Configuration Time	-	50ms

SPI Timing



Symbol	Description	Min	Max	Units
Fsck	SCLK Clock Frequency	-	80	MHz
TWH	SCLK High duration	6	-	ns
TWL	SCLK Low duration	6	-	ns
TCS	nSCS High duration	5	-	ns