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WIZ550io

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Overview

WIZ550io is an auto configurable Ethernet controller that includes a W5500 (TCP/IP hardwired chip and PHY embedded), a transformer and RJ45.

It has a unique real MAC address and configures the network setting automatically. When powered on, WIZ550io initializes itself ... with embedded real MAC and sets the default IP address (192.168.1.2) and it can be pinged. Therefore, users are not required to write MAC and network information like IP address, Subnet mask and Gateway address. The WIZ550io is an ideal product for users who want to develop their Internet enabling systems rapidly.

For more information on the W5500 chip inside the WIZ550io module please also refer to the chip's datasheet:

Datasheet

- W5500 Datasheet v1.0.9 - English
- W5500 Datasheet v1.0.9 - Korean

Datasheet History

Version	Date	Description
1.0.0	2013-08-01	Initial Release
1.0.1	2013-09-13	Corrected duplicated statements and typing errors (P.14, 23, 24, 28, 39, 51) Corrected descriptions (P.35)
1.0.2	2013-11-14	Changed *"descriptions of pin at 1.1 Pin Descriptions"* (P.10) starting "It must be tied to GND to NC (PIN38..42)" / 2. corrected typing error: starting "0x02 to 0x42 value of SOCK_MACRAW at 4.2 Socket Registers(P.50)"
1.0.3	2014-05-29	Corrected *"Sn_MSSR at 4.2 Socket Register"* (P.53): wrong descriptions of Sn_MSSR about FMTU/MTU
1.0.4	2014-06-13	1. Added Note about reading size register value (P.56, 58) / 2. Added IR Reflow Temperature Profile (P.66)

Version	Date	Description
1.0.5	2014-11-11	1. Added description for MISO pin (P.11):The SCSn signal defines MISO pin output value / 2. Modified the register notation (P.33), Modified the register notation “Sn_IR at 4.2 Socket Register” (P.49) :from [R] to [RCW1] / 3. Corrected typing error: from DICON to DISCON of Sn_SR at 4.2 Socket Register (P.50)
1.0.6	2014-12-30	Corrected typing error : from 0x02 to 0x42 value of SOCK_MACRAW *“Sn_CR at 4.2 Socket Registers”*(P.46)
1.0.7	2016-02-24	1. Corrected Interrupt Assert Wait Time function (P.34) / 2. Notice PLLclk is 150MHz (P.34)
1.0.8	2017-05-19	1. Corrected Driver Level Range Unit uW/MHz to uW (P.60)
1.0.9	2019-05-22	1. Corrected Sn_IMR Description (P.55) 2. Corrected Junction temperature Min value TJ (P.57) 3. Added Maximum junction temperature TJMAX (P.58)

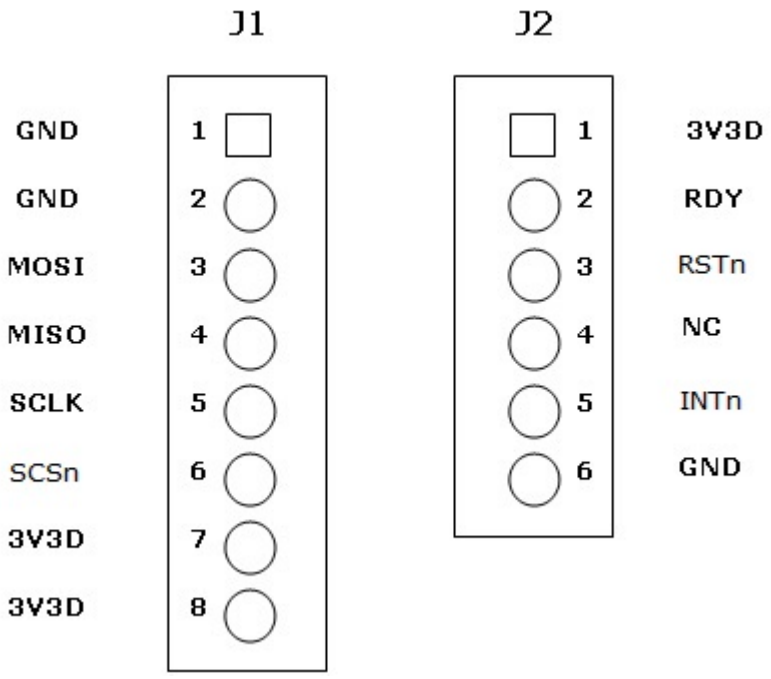
WIZ550io History

Version	Date	Description
1.0	2013-08-01	Initial Release
1.1	2014-01-17	Changed *“External Transformer + RJ-45 to MAGJACK(inside transformer)”*
1.2	2015-04-20	Added *“Resistor 33R in MDI line. because EMI issue.”* Changed *“PCB artwork. because changed develop tool(PADS → Altium) ”*
1.3	2018-08-10	Modified *“inner 2 layer copper foil (3V3D). This copper foil plated below of CHAND area. It may affect ESD.”*

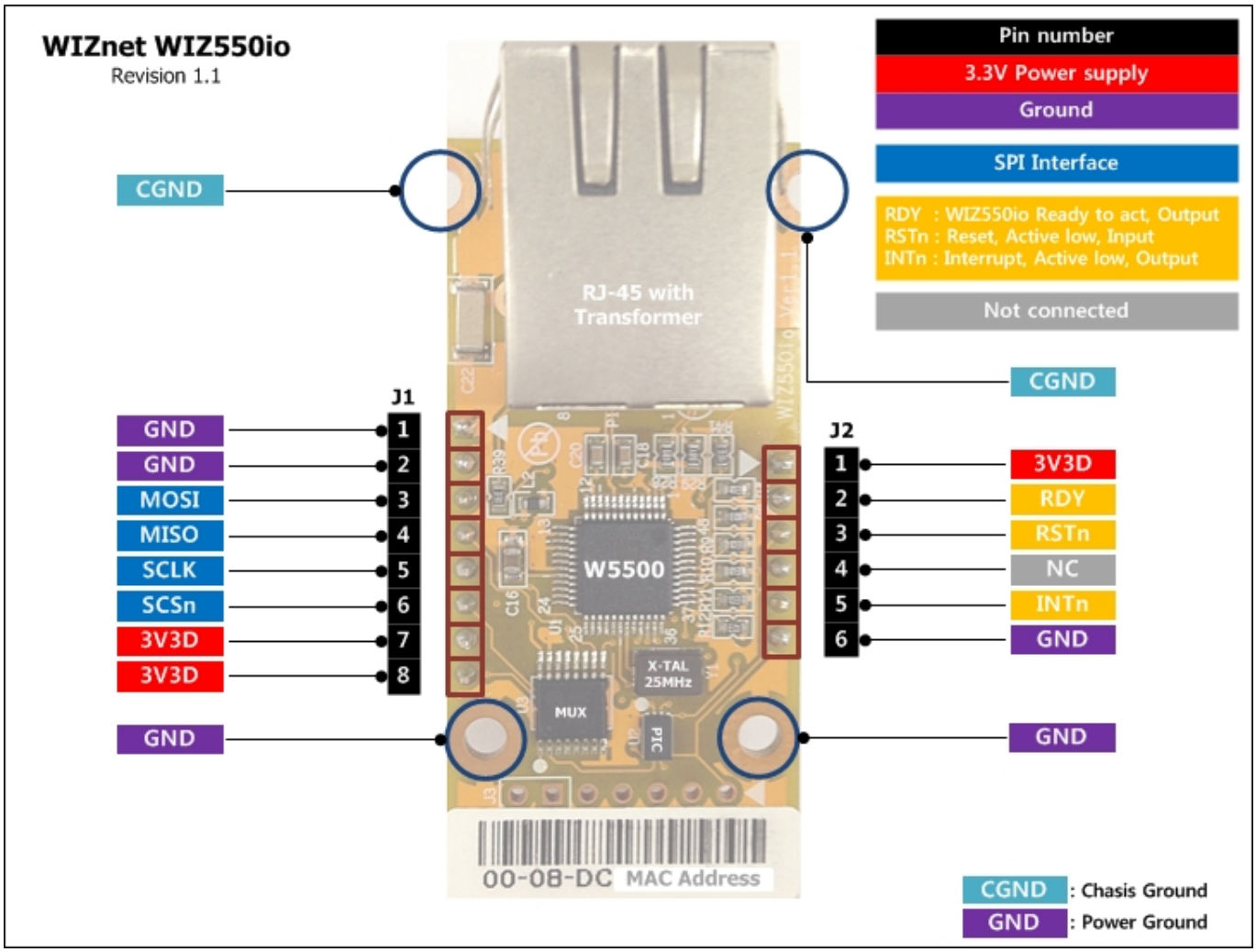
2013/08/30 10:01 · bongbong
2013/08/28 09:00 · jameskim

Hardware Pins of WIZ550io

Pin Map



Pin out



Revision 1.2 version pinout is same to revision1.1 version.

Pin Description

Pin No.		I/O	Pin Name	Description
J1	1	P	GND	**Ground**
	2	P	GND	**Ground**
	3	I	MOSI	**SPI Master Out Slave In** This pin is used for SPI MOSI signal pin
	4	O	MISO	**SPI Master In Slave Out** This pin is used for SPI MISO signal pin
	5	I	SCLK	**SPI Clock** This pin is used for SPI Clock Signal pin
	6	I	SCSn	**SPI Slave Select** This pin is used for SPI Slave Select Signal Pin when using SPI interface
	7	P	3V3D	**Power**: 3.3V Power Supply
	8	P	3V3D	**Power**: 3.3V Power Supply

Pin No.		I/O	Pin Name	Description
J2	1	P	3V3D	**Power**: 3.3V Power Supply
	2	O	RDY	**READY** This pin is asserted to low after power on. When RSTn is activated, WIZ550io does auto configuration with embedded MAC and default IP address. After configuration gets completed, WIZ550io raises this pin to HIGH in order to inform about the completion of WIZ550io's configuration. Host processor can only control WIZ55oio when RDY pin is HIGH.
	3	I	RSTn	**Reset**: Low activity This pin is to initialize WIZ550io. Hold at least 500us after asserted to LOW and wait for at least 150ms after it is changed to HIGH until WIY550io configured itself.
	4	I	NC	**Not Connected**
	5	O	INTn	**Interrupt**: Low activity This pin indicates that W5500 inside WIZ550io requires MCU's due to events like socket connection, disconnection, data receiving timeout and WOL (Wake on Lan). The interrupt is cleared by writing IR register or Sn_IR. All interrupts are maskable.
	6	P	GND	**Ground**

Caution)
Some users may want to reinitialize W5500 inside WIZ550io with SW reset, not handling RSTn pin. It will make WIZ550io hang up due to clearance of all information in the registers of W5500. A tiny MCU inside WIZ550io initializes W5500 with embedded MAC address and a default IP address and Initialization is triggered by RSTn.

In case of SW reset, all registers in W5500 will be cleared and WIZ550io will not initialize itself. All information inside WIZ550io will be lost and WIZ550io will hang up instead.

Therefore, we recommend HW reset instead of SW reset. Nevertheless, if users want to use SW reset, we recommend to save MAC address and network information including IP address, Subnet mask and Gateway address before SW reset, and writing those information to WIZ550io after SW reset.

2013/08/28 09:08 · jameskim

Characteristic

DC Charcteristic

Symbol	Parameter	Pins	Min	Typ	Max	Unit
VDD	**Supply voltage**	3.3V	2.97	3.3	3.63	V
VIH	**High level input voltage**	ALL	0.7*Vcc		5.5	V
VIL	**Low level input voltage**	ALL	-0.3		0.3*Vcc	V
VOH	**High level output voltage**	ALL	2.9	3.3		V
VOL	**Low level output voltage**	ALL	0.0		0.52	V
IDD	**Supply Current (Normal operation mode)**	3.3V		141		mA
LOH	**Supply Current (Power Down mode)**	3.3V		13		mA

Power Dissipation

Condition	Min	Typ	Max	Unit
100M Link	-	135	-	mA
10M Link	-	80	-	mA
Unlink (Auto-negotiation mode)	62	-	75	mA
100M Transmitting	137	-	141	mA
10M Transmitting	-	83	-	mA
Power Down mode	-	13	-	mA

2016/03/04 19:30 · jameskim

SPI Operations

There is a W5500 inside WIZ550io. Therefore SPI operation of WIZ550io follows one of W5500. For more information about SPI operation of WIZ550io, please refer to W5500 Datasheet.

Datasheet

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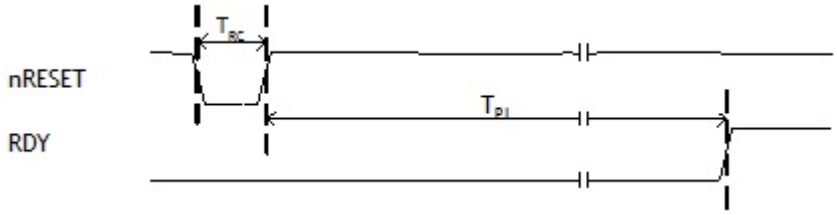
2013/08/28 09:12 · jameskim

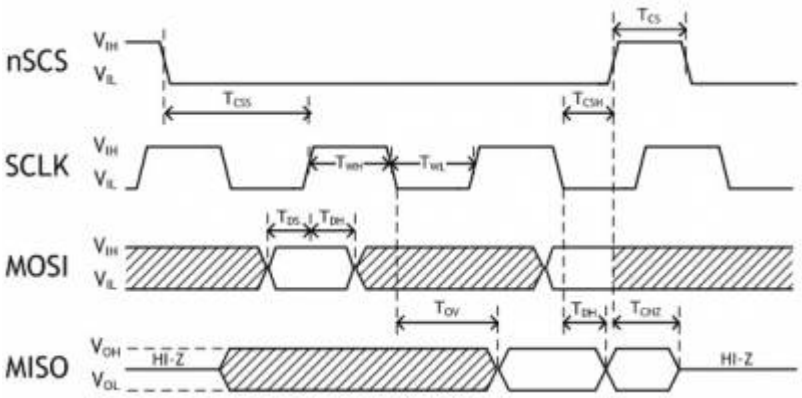
Timing Diagram

Reset Timing



Symbol	Description	Min	Max
TRC	Reset Cycle Time	500us	-
TPL	Internal Auto Configuration Time	-	50ms

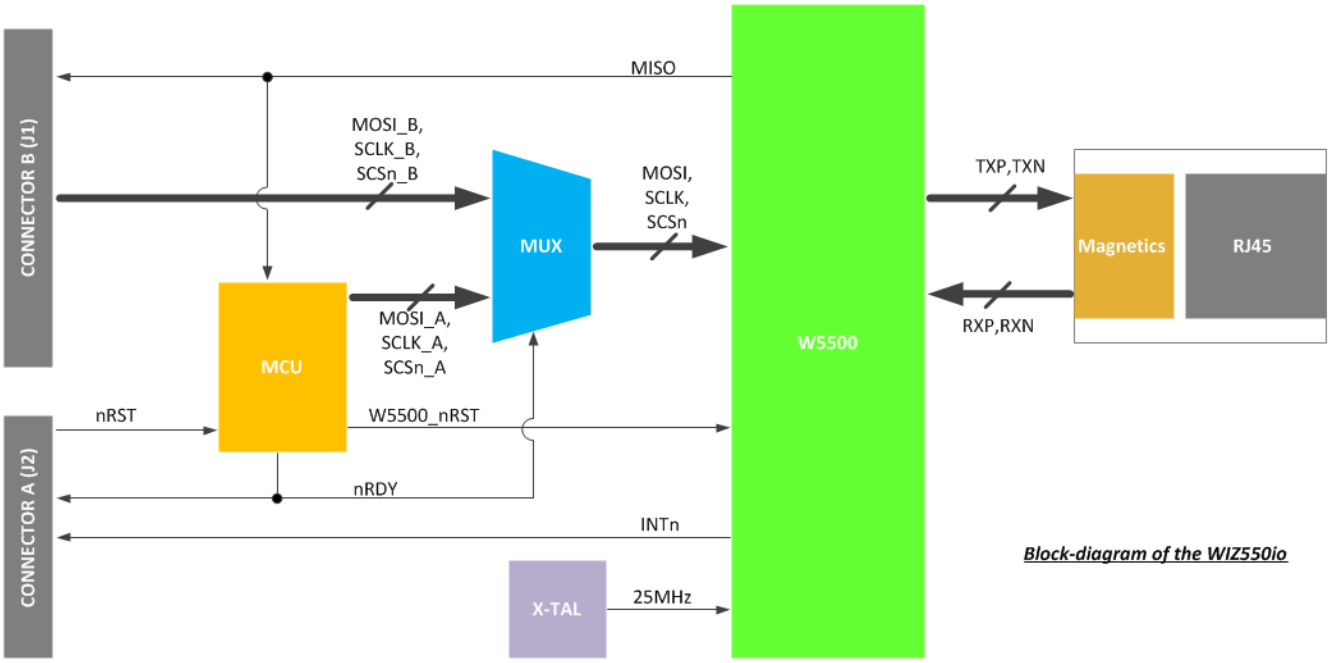
SPI Timing



Symbol	Description	Min	Max	Units
Fsck	SCLK Clock Frequency	-	80	MHz
TWH	SCLK High duration	6	-	ns
TWL	SCLK Low duration	6	-	ns
TCS	nSCS High duration	5	-	ns

2013/08/28 09:13 · jameskim

Block Diagram



Block-diagram of the WIZ550io

Schematic

- Revision 1.0 WIZ550io Rev1.0 Schematic
- Revision 1.1 WIZ550io Rev1.1 Schematic
- Revision 1.2/1.3 WIZ550io Rev1.2/1.3 Schematic

PCB

- Revision 1.2
  WIZ550io Rev1.2 PCB(Altium)
- Revision 1.3
  WIZ550io Rev1.3 PCB(Altium)

Partlist

- Revision 1.0 Partlist WIZ550io Rev1.0 Partlist
- Revision 1.1 Partlist WIZ550io Rev1.1 Partlist
- Revision 1.2 Partlist WIZ550io Rev1.2 Partlist

2014/02/07 15:38 · peter.kim

Dimension

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WIZ550io Ver1.0
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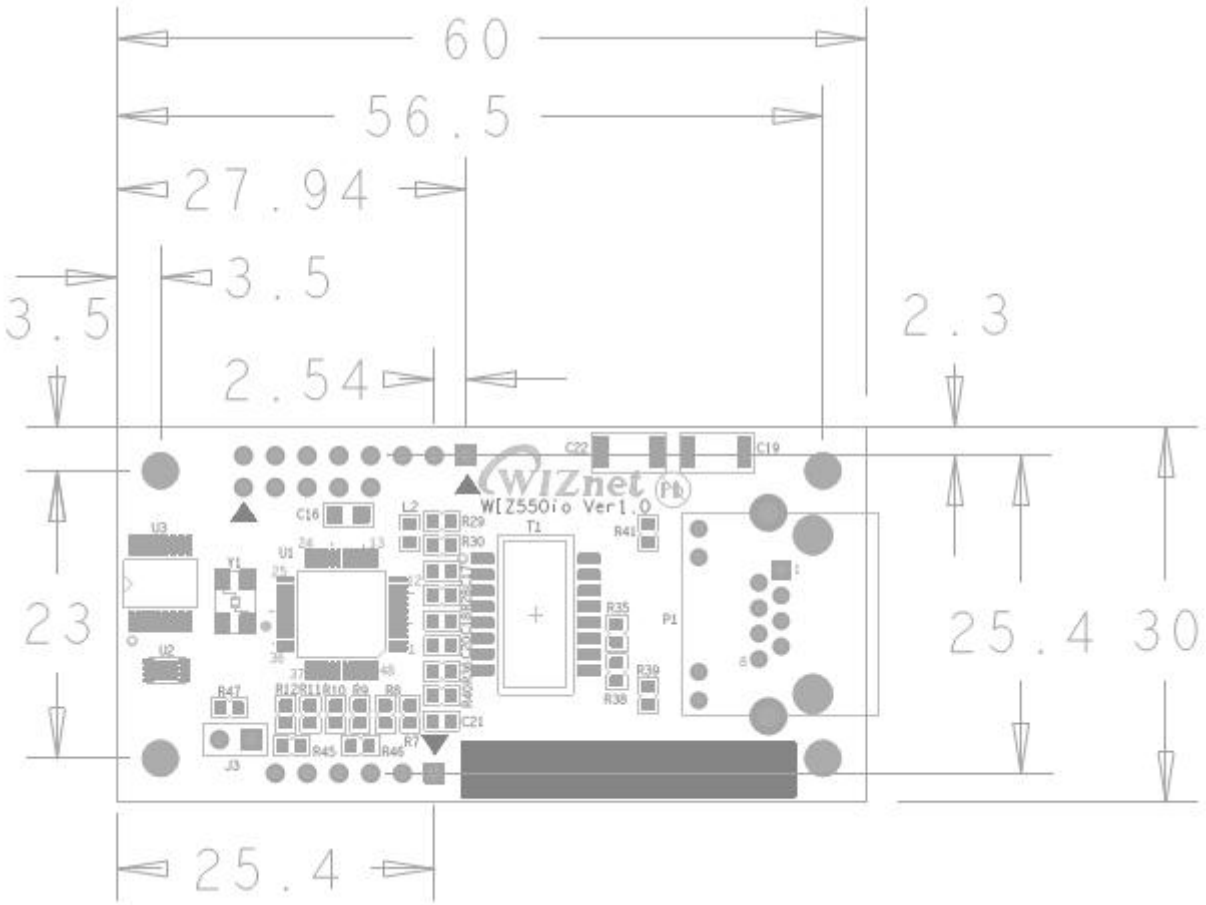
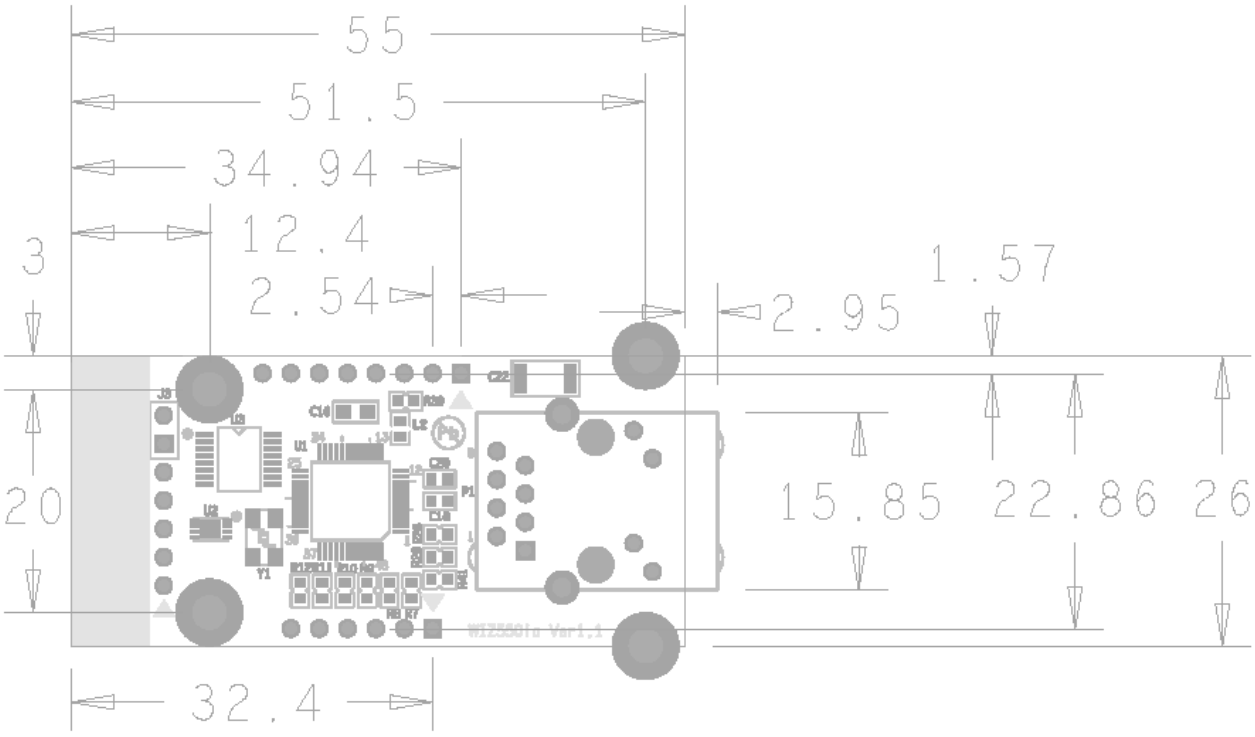


WIZ550io Ver1.1

54mm(W) x 26mm(L) x 24mm(H) (±0.5)

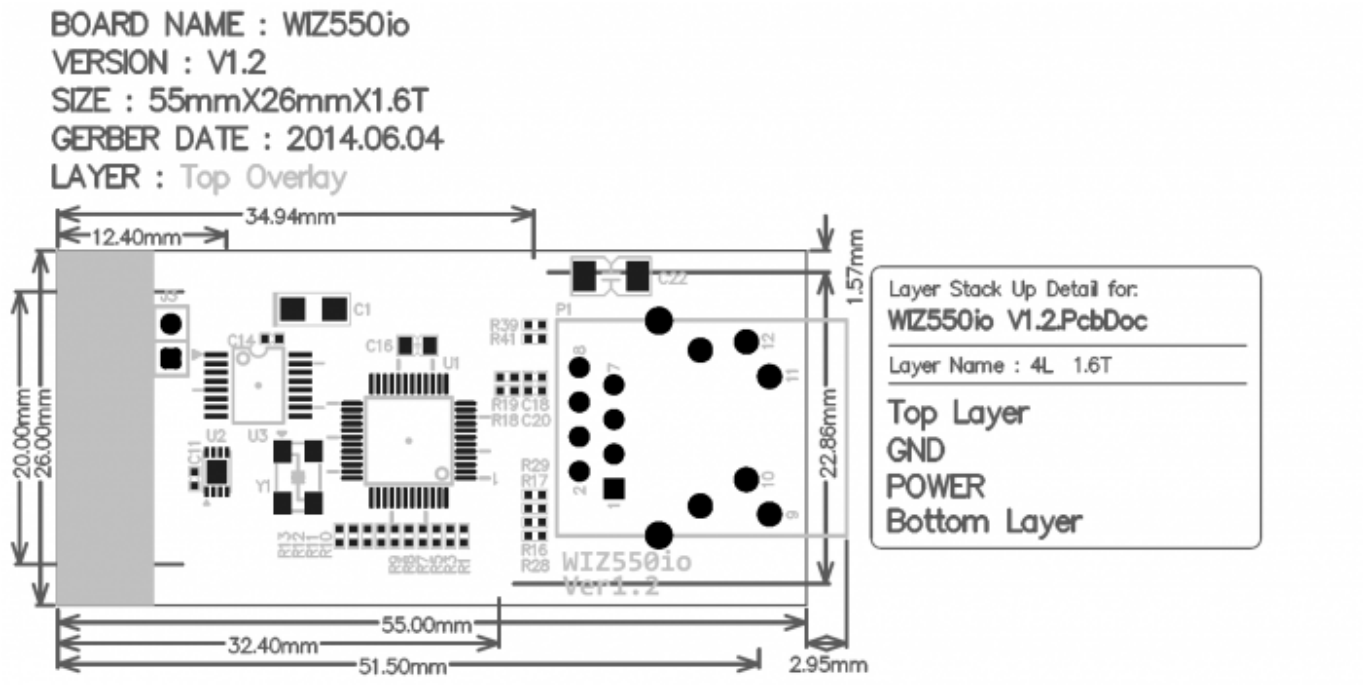


WIZ550io Ver1.2

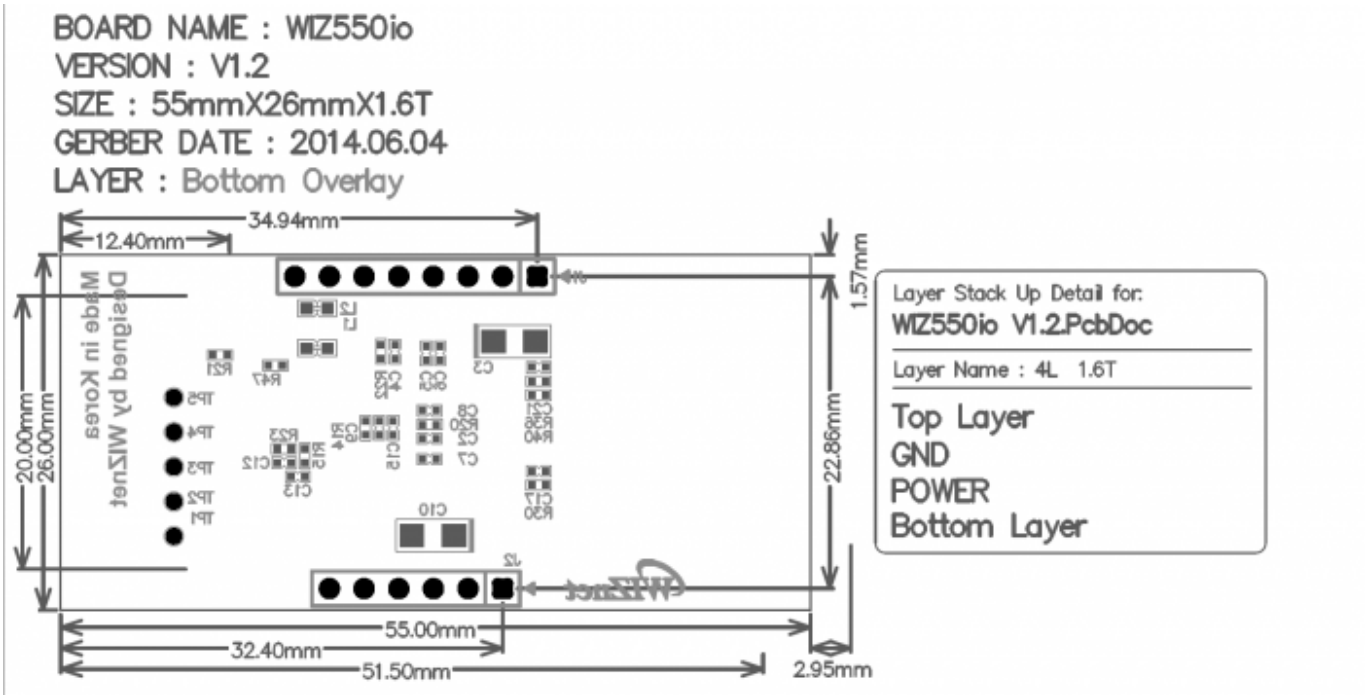
54mm(W) x 26mm(L) x 24mm(H) (±0.5)

Same to Ver1.1 and Ver1.2 PCB all size and hole size. There is little change in all parts placement.

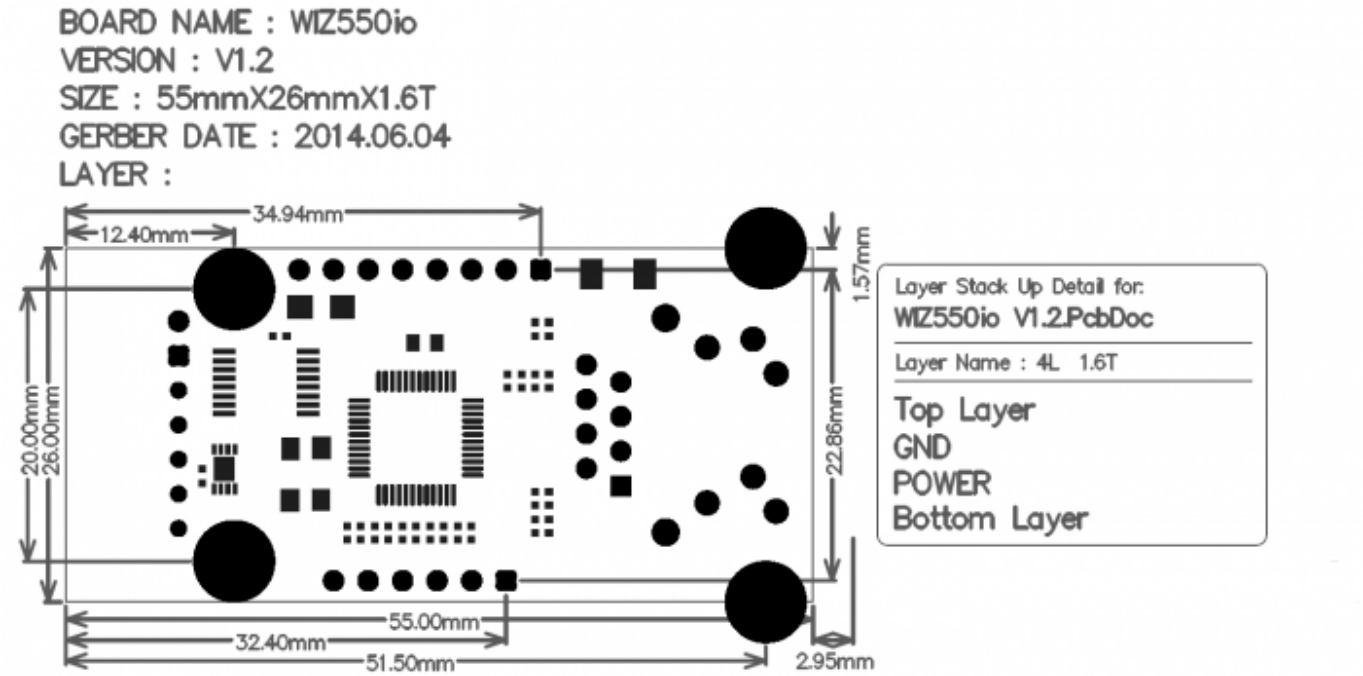
* TOP



* BOTTOM



* Drill



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Related Products

- ioShield-A
- ioShield-K
- ioShield-L

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