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W7500P



The IOP4IoT W7500P chip is the one-chip solution which integrates an ARM Cortex-M0, 128KB Flash, hardwired TCP/IP core for various embedded application platform, 10/100 Ethernet MAC and PHY, and especially internet of things. The TCP/IP core is a market-proven hardwired TCP/IP stack and PHY is IC plus IP101G, an IEEE 802.3/802.3u Fast Ethernet Transceiver for 10/100Mbps. The Hardwired TCP/IP stack supports the TCP, UDP, IPv4, ICMP, ARP, IGMP and PPPoE which has been used in various applications for more than 15 years. W7500P suits users who need Internet connectivity best.

Features

- ARM Cortex-M0
 - 48MHz maximum frequency
- Hardwired TCP/IP Core
 - 8 Sockets
 - SRAM for socket: 32 KB
- PHY
 - IC+(IP101G)
- Memories
 - Flash: 128 KB
 - SRAM: 16KB
 - ROM for boot code: 6 KB
- Clock, reset and supply management
 - POR (Power-On Reset)
 - Internal Voltage Regulator : 3.3V to 1.5V
 - 8-to-24MHz external crystal oscillator
 - Internal 8MHz RC Oscillator
 - PLL for CPU clock
- ADC : 12bit, 8ch, 1Msps
- DMA
 - 6-channel DMA controller
 - Peripheral supported: UARTs, SPIs
- GPIO
 - 34 I/Os (15 IO x 2ea, 4 IO x 1ea)
- Debug mode
 - Serial Wire Debug (SWD)
- Timer/PWM
 - 1 Watchdog (32-bit down-counter)
 - 4 Timers (32-bit or 16-bit down-counter)
 - 8 PWMs (32-bit counter/timers with programmable 6-bit prescaler)
- Communication Interfaces
 - 3 UART (2 UARTs with FIFO and Flow Control, 1 simple UART)
 - 2 SPI
 - 2 I2C (Master/Slave, Fast-mode (400 kbps))
- Crypto
 - 1 RNG (Random Number Generator): 32-bit random number

- Package
 - 64 LQFP (7x7 mm)

Details

- [Pin Assignment](#)
- [System and Memory](#)
- [Interrupt and Events](#)
- [Power supply](#)
- [Booting Sequence](#)
- [Electrical Characteristics](#)
- [W7500P Ref.Schematic](#)

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Peripheral description and examples

Peripheral	Example
GPIO	Blink_LED
ADC	Illumination RGB LED
DMA	Memory to memory copy
CRG	
DualTimer	TimerRun
EXTI	LED_Toggle, Sleep
Flash	IAP Example
I2C	Default, EEPROM 24LS02, Temperature LM75
PWM	CaptureMode, CounterMode, DeadZoneGeneration, PWMOutput, TimerMode
RNG	Random number generation example
SSP	Loopback, SD Card LED
TOE	Loopback, DHCP, DNS
UART	Interrupt, Polling, Printf, Uart Hardware Flow Control
WDT	WDTReset
SysTick	Delay example
AFC	
PADCON	

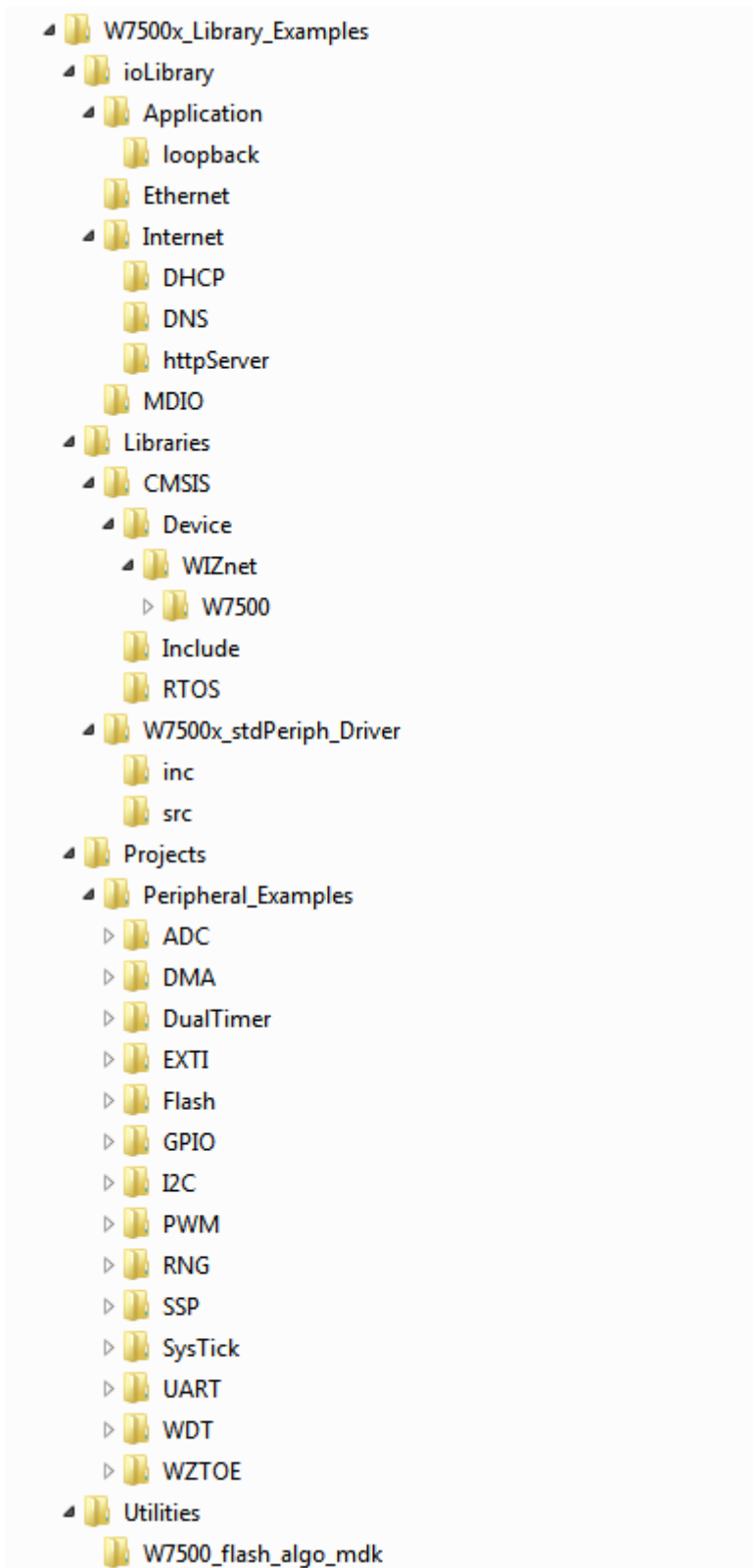
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Library and Peripheral Example

Overview

The W7500P provides the CMSIS, driver and Peripheral Example. The W7500P Standard Peripherals library provides a rich set of examples covering the main features of each peripheral. All the examples are independent from the WIZwiki-W7500P platform. Only source files are provided for each example and user can tailor the provided project template to run the selected example with his preferred tool chain.

- Directory Structure



- ioLibrary
 - Application
 - loopback
 - Ethernet
 - Internet
 - DHCP
 - DNS
 - httpServer
 - MDIO
- Libraries

- CMSIS :CMSIS Library
- W7500x_stdPeriph_Driver
 - Each peripheral has a source code file W7500x_XXX.c and a header file W7500x_XXX.h. The W7500x_XXX.c file contains all the firmware functions required to use the XXX peripheral.
 - A single memory mapping file, W7500x.h, is supplied for all peripherals. It contains all the register declarations and bit definition. This is the only file that needs to be included in the user application to interface with the library.
- Projects
 - peripheral_Examples
 - The W7500P standard Peripherals library provides a rich set of examples covering the main features of each peripheral.
- Utilities
 - w7500p_flash_algo_mdk
 - The W7500P standard library provides W7500P 128KB flash algorithm project to debug WIZwiki-W7500P with using ULINK debugger and CMSIS-DAP debugger.

Download

Library GitHub Repository

Release Version

- [W7500P Github Release Version List](#)

Peripheral description and examples

- [Peripherals](#)

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