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Power supply

Introduction

W7500 embeds a voltage regulator in order to supply the internal 1.5V digital power domain.

- Require a 2.7V ~ 5.5V operating supply voltage (VDD)
- ADC ref voltage is same as VDD

Voltage regulator

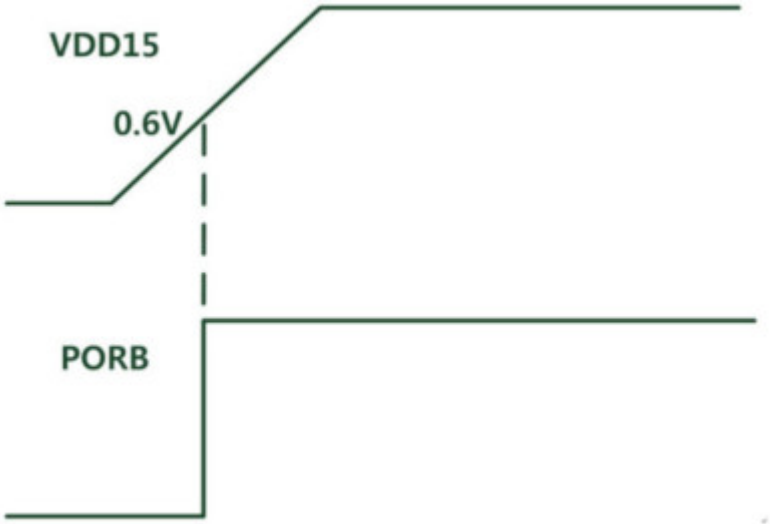
The voltage regulator is always enabled after Reset and works on in only one mode.

- In Run mode, the regulator supplies full power to the 1.5V domain.
- There is no power down or sleep mode.

Power supply supervisor

W7500 has an integrated reset (POR) circuit which is always active and ensure proper operation above a threshold of 0.6V

- The POR monitors only the VDD supply voltage. During the startup phase VDD must arrive first and be greater than or equal to 0.6V



Low power modes

W7500 is in RUN mode after a system or power reset. There are two low power modes to save power when the CPU does not need to be kept running. These modes are useful for instances like when the CPU is waiting for an external interrupt. Please note that there is no power-off mode for W7500.

The device features two low power modes:

- Sleep mode
- Deep Sleep mode

Additionally, the power consumption can be reducing by following method:

- User can slow down the system clocks
- User can block the clocks to the peripherals while they are unused.

Sleep mode vs. Deep sleep mode

W7500 has two kinds of sleep modes. One is Sleep mode and the other is Deep sleep mode. Two of them are almost the same except the clock gated peripherals kinds.

Mode	Entry	Wakeup	Effect-on-clocks
Sleep mode	DEEPSLEEP = 0 Enable WFI	Any interrupt	CPU Clock OFF APB Bus Clock ON AHB Bus Clock ON Memory Clock ON
	DEEPSLEEP = 0 Enable WFE	Wakeup event	
Deep Sleep mode	DEEPSLEEP = 1 Enable WFI	Any interrupt	CPU Clock OFF APB Bus Clock OFF AHB Bus Clock OFF Memory Clock OFF
	DEEPSLEEP = 1 Enable WFE	Wakeup event	

Peripheral clock gating

In Run mode, individual clocks can be stopped at any time to reduce power. Peripheral clock gating is controlled by the CRG block. Below is the list of clocks which can be gating in CRG block.

- ADC clock (ADCCLK)
- SSP0, SSP1 clock (SSPCLK)
- UART0, UART1 clock (UARTCLK)
- Two Timer clocks (TIMCLK0, TIMCLK1)
- 8 PWM clocks (PWMCLK0 ~ PWMCLK7)
- WDOG clock (WDOGCLK)
- Random number generator clock (RNGCLK)