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virtual W7100A datasheet - under construction

Overview

Introduction

iMCU **W7100A** is the one-chip solution which integrates an 8051 compatible microcontroller, 64KB SRAM and hardwired TCP/IP Core for high performance and easy development. The TCP/IP core is a market-proven hardwired TCP/IP stack with an integrated Ethernet MAC & PHY. The Hardwired TCP/IP stack supports the TCP, UDP, IPv4, ICMP, ARP, IGMP and PPPoE which has been used in various applications for years.

W7100A Features

- Fully software compatible with industrial standard 8051
- Pipelined architecture which enables execution of instructions 4~5 times faster than a standard
- 8051
- 10BaseT/100BaseTX Ethernet PHY embedded
- Power down mode supported for saving power consumption
- Hardwired TCP/IP Protocols: TCP, UDP, ICMP, IPv4 ARP, IGMP, PPPoE, Ethernet
- Auto Negotiation (Full-duplex and half duplex), Auto MDI/MDIX
- ADSL connection with PPPoE Protocol with PAP/CHAP Authentication mode support
- independent sockets which are running simultaneously
- 32Kbytes Data buffer for the Network
- Network status LED outputs (TX, RX, Full/Half duplex, Collision, Link, and Speed)
- Not supports IP fragmentation (driver function)
- 2 Data Pointers (DPTRs) for fast memory blocks processing
- Advanced INC & DEC modes
- Auto-switch of current DPTR
- 64KBytes Data Memory (RAM)
- 255Bytes data FLASH
- 64KBytes Code Memory
- 2KBytes Boot Code Memory
- Up to 16M bytes of external (off-chip) data memory (100pin version)
- Interrupt controller
- 2 priority levels
- 4 external interrupt sources
- Watchdog interrupt
- Four 8-bit I/O Ports
- Three timers/counters
- Full-duplex UART (max. 230kBaud)
- Programmable Watchdog Timer
- DoCD™ compatible debugger
- High Product Endurance
- Minimum 100,000 program/erase cycles (FLASH)
- Minimum 10 years data retention

W7100A Datasheet

Datasheet History

Version	Date	Description
0.9.1	2011-Sept.	Initial beta

Version	Date	Description
...	2011-2013	many versions
1.2.2	2013-Jun.	Added “recommendation of watchdog timer interrupt at 7.4 Simple Timer”(P.69)

Link to WIZnet product page:
http://eucache.wiznet.co.kr/sub_modules/en/product/product_detail.asp?Refid=667&page=1&cate1=5&cate2=40&cate3=55&pid=1131&cType=2
→ Download → Datasheet

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some shortcut Links into the 'virtual' datasheet

- W7100A Block Diagram & Features
- Pin Description
- Code Memory
- Data Memory
- external Memory (100pin)
- internal Data Memory & SFR
- SFR definition
- Interrupt
- I/O Ports
- Timers 0,1
- Timer 2
- UART
- Watchdog
- TCP/IP Core
  - Memory Map
  - Registers List
  - Register Description
  - Initialization
  - Data Communication
  - TCP Server/Client
  - UDP
  - IPRAW
  - MACRAW
- Electrical Specification
- Package & IR Reflow Temp. Profile
- 8-Bit Arithmetic Functions
- 16-Bit Arithmetic Functions
- 32-Bit Arithmetic Functions
- ISP Flash Programming protocol

The virtual W7100A Datasheet - Start (does not exist yet)