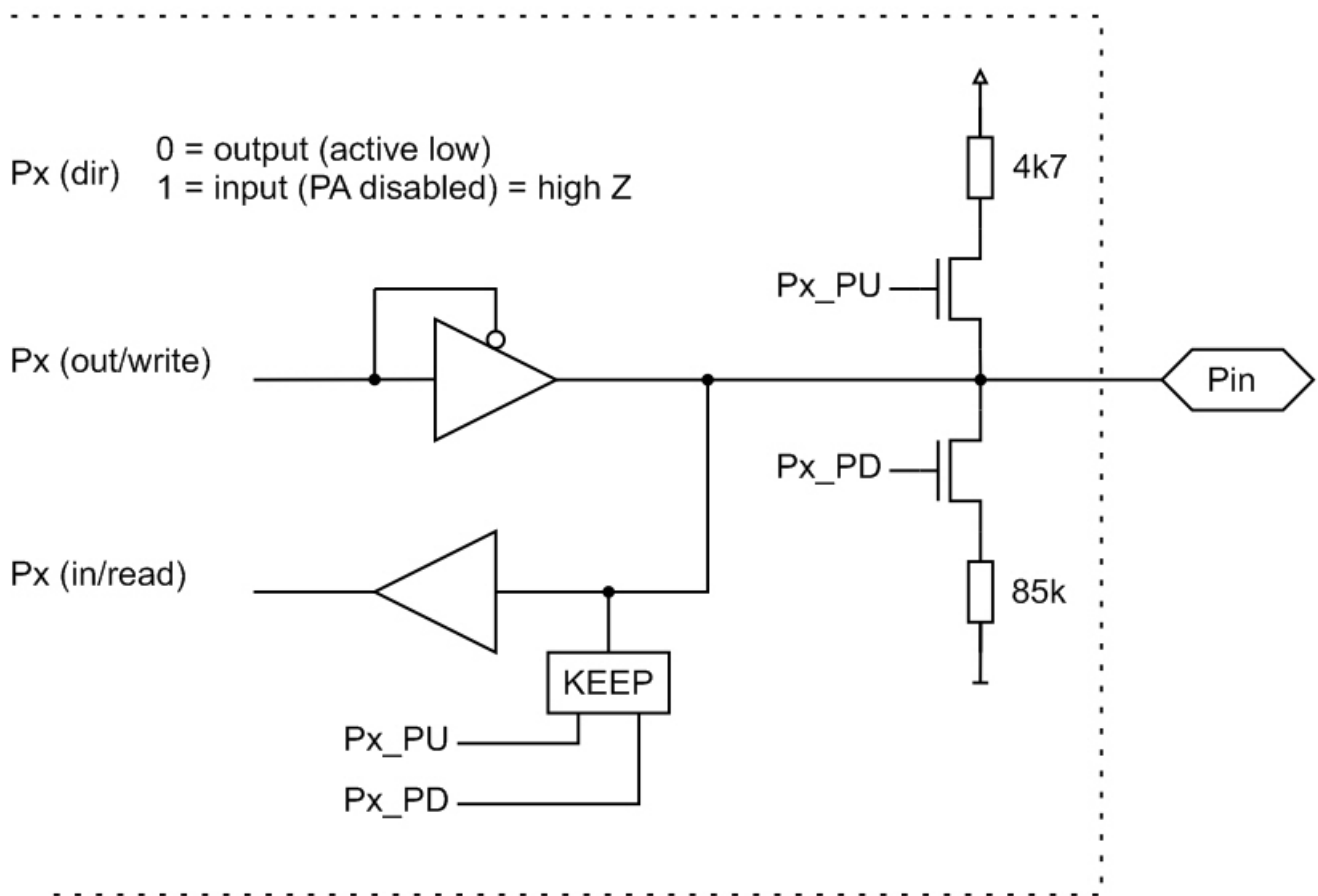


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## I/O Ports , P0, P1, P2, P3



The GPIO of the **W7100A** MCU has five operating modes, 'active low', 'high Z', 'Pull-up', 'Pull-down' and 'Keep' according to the SFR values. The output driver is a simple open drain stage and not a Push-Pull output. Therefore a low-impedant 'high' to the output must be performed with the internal 4k7 pull-up resistor.

With the port registers Px the direction (in or out) of the port pins is selected.

With the registers Px\_PD and Px\_PU the internal Pull-Down and Pull-Up resistors are activated.

The 'Keep' mode can be made by setting up both pull-up and pull-down register simultaneously.

The GPIO port register keeps its previous value in the 'Keep' operating mode until leaving Keep-Mode.

The I/O port pin functionalities are described in the following table:

### I/O Ports Pin Description

Pin	Active	Type	Pu/Pd	Description
P0[7:0]	-	IO	-	Port0 input / output
P1[7:0]	-	IO	-	Port1 input / output
P2[7:0]	-	IO	-	Port2 input / output
P3[7:0]	-	IO	-	Port3 input / output

Some port-reading instructions read from the data registers while others read from the port pin.

The "Read-Modify-Write" instructions are directed to the data registers as shown below.

## Read-Modify-Write Instructions (register access)

Instruction	Function Description
ANL	Logic AND
ORL	Logic OR
XRL	Logic exclusive OR
JBC	Jump if bit is set and cleared
CPL	
INC, DEC	Increment, decrement byte
DJNZ	Decrement and jump if not zero
MOV Px.y, C	Move carry bit to bit y of port x
CLR Px.y	Clear bit y of port x
SETB Px.y	Set bit y of port x

All other instructions read from a port exclusively through the port pins. All port pins can be used as GPIO (General Purpose Input Output). The output driving voltage of the GPIO is 0V or 3.3V according to the Px\_PD and Px\_PU SFR value or the GPIO keeps its previous value in current operation mode.

Read and write accesses are performed in the I/O ports via their corresponding SFR: P0 (0x80), P1 (0x90), P2 (0xA0), and P3 (0xB0).

Px Status	
0	output
1	input (tri-state)

Internal pull-down (85k) and pull-up (4k7) resistors are activated by Px\_PD (0xE3..0xE6) and Px\_PU (0xEB..0xEE) register.

Px_PU	Px_PD	Status
0	0	-
0	1	Pull-down
1	0	Pull-up
1	1	Keep mode

### Use case: Output

For best output performance activate Px\_PU (4k7 pull-up) and use direction register Px to set the port pin to 0 or 1.

direct.	Px	Px_PD	Px_PU	out	annotation
out	0	0	0	0	low imp. (no internal current)
		0	1	0	low imp. (0.7mA current in 4k7)
'in'	1	0	1	1	4k7 pull-up

### Use case: Input

For best input performance write '1' into the Px register. This will make the port pin high impedant and set input direction. Additionally and if needed activate the internal resistors with the Px\_PD or Px\_PU registers corresponding to your external circuit.

A read operation on the Px register is done directly to the Port Pin status.

direct.	Px	Px_PD	Px_PU	in	annotation
in	1	0	0	-	high imp. - tri-state (2.5V)
		0	1	1	4k7 pull-up
		1	0	0	85k pull-down
		1	1	-	Keep mode

## All peripheral registers:

### P0 (0x80)

7	6	5	4	3	2	1	0	Reset value
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	0xFF

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### P1 (0x90)

7	6	5	4	3	2	1	0	Reset value
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	0xFF

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### P2 (0xA0)

7	6	5	4	3	2	1	0	Reset value
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	0xFF

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### P3 (0xB0)

7	6	5	4	3	2	1	0	Reset value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	0xFF

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### P0\_PU (0xEB):

7	6	5	4	3	2	1	0	Reset value
Port0[7]	Port0[6]	Port0[5]	Port0[4]	Port0[3]	Port0[2]	Port0[1]	Port0[0]	0x00

GPIO0 **Pull-up** register, the value '1' means the internal 4k7 pull-up resistor of the related pin is activated.

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